What is claimed is:

1. A method of trench isolation comprising:

forming a first oxide layer on a semiconductor substrate;

successively forming a first conductive layer and a nitride layer on the first oxide layer;

etching the nitride layer, the first conductive layer and the first oxide layer to form a nitride layer pattern, a first conductive layer pattern and an oxide layer pattern;

etching a portion of the substrate adjacent to the first conductive layer pattern to form a trench in the substrate;

curing the trench using a compound including nitrogen;

forming a second oxide layer on a bottom and a sidewall of the trench; and

forming a field oxide layer to fill up the trench.

2. The method of claim 1, wherein the trench is formed through a self-alignment process using the nitride layer pattern as a mask.

3. The method of claim 2, wherein the first conductive layer pattern and the oxide layer pattern are formed using the nitride layer pattern as the mask.

4. The method of claim 1, wherein the compound includes at least one of dinitrogen monoxide (N_2O) and nitrogen monoxide (NO).

5. The method of claim 1, wherein curing the trench is performed through an annealing process at a temperature of above about 800°C.

6. The method of claim 5, wherein the second oxide layer is formed through an in-situ process.

7. The method of claim 6, wherein the second oxide layer is formed at a temperature of about 700°C to about 800°C.

8. The method of claim 1, wherein the second oxide layer includes medium temperature oxide.

9. The method of claim 8, wherein the second oxide layer has a thickness of about 140Å to about 160Å.

10. The method of claim 1, wherein forming the field oxide layer comprises:

forming a third oxide layer to fill up the trench and to cover the nitride layer pattern; and

planarizing the third oxide layer through a chemical mechanical polishing (CMP) process or an etch-back process to expose an upper face of the nitride layer pattern.

11. The method of claim 10, wherein the third oxide layer includes at least one of borophosphosilicate glass (BPSG), ozone-tetraethylorthosilicate (O_3-TEOS),

undoped silicate glass (USG) and high density plasma (HDP) oxide.

12. A method for manufacturing a non-volatile memory device comprising:

forming a first oxide layer on a semiconductor substrate;

forming a first conductive layer on the first oxide layer;

forming a nitride layer on the first conductive layer;

etching the nitride layer, the first conductive layer and the first oxide layer to form a nitride layer pattern, a first conductive layer pattern and an oxide layer pattern;

etching a portion of the substrate adjacent to the first conductive layer pattern using the nitride layer pattern as a mask to form a trench in the substrate;

curing the trench using a compound including nitrogen;

forming a second oxide layer on a bottom and a sidewall of the trench through an in-situ process;

forming a third oxide layer to fill up the trench and to cover the nitride layer pattern;

removing the third oxide layer to form a field oxide layer in the trench;

forming a second conductive layer pattern on the first conductive layer pattern; and

successively forming an oxide/nitride/oxide layer and a third conductive layer on the second conductive layer pattern.

13. The method of claim 12, wherein the trench is formed through a self-alignment process using the nitride layer pattern as a mask.

14. The method of claim 12, wherein the compound includes at least one of dinitrogen monoxide (N_2O) and nitrogen monoxide (NO).

15. The method of claim 12, wherein curing the trench is performed through an annealing process at a temperature of above about 800°C.

16. The method of claim 12, wherein the second oxide layer having a thickness of about 140Å to about 160Å includes medium temperature oxide.

17. The method of claim 16, wherein the second oxide layer is formed at a temperature of about 700°C to about 800°C.

18. The method of claim 12, wherein the first and second conductive patterns correspond to a floating gate, and the third conductive layer corresponds to a control gate.

19. The method of claim 12, wherein, prior to forming the second conductive layer pattern, the third oxide layer is planarized through an etch-back process or a chemical mechanical polishing (CMP) process to expose an upper face of the nitride layer pattern, and the nitride layer pattern is selectively removed to expose an upper face of the first conductive layer pattern.

20. The method of claim 12, wherein, prior to forming the second conductive

layer pattern, the third oxide layer is planarized through an etch-back process or a chemical mechanical polishing (CMP) process to expose an upper face of the first conductive layer pattern.

21. The method of claim 12, wherein the third oxide layer includes at least one of BPSG, O_3-TEOS, USG and high density plasma (HDP) oxide.